Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the Claims:

Claim 1. (Currently Amended) An image sensor comprising:

a plurality of pixels each having an output, each pixel including:

a first circuit that produces a signal proportional to incident light intensity, said first circuit being connected to supply said proportional signal to said pixel output,

a select node connected to receive a select signal for selecting said pixel from said plurality of pixels, and

a reset transistor for resetting said pixel;

an amplifier having:

a first input for receiving said outputs of said pixels, and

an output connected to said pixels to be actively coupled to said reset transistors during a pixel reset phase to provide a negative feedback signal to a selected pixel during said pixel reset phase; and

a reset reference voltage source connected to apply a reset reference voltage signal to said amplifier to provide a voltage reference for controlling reset of said pixels.

Claim 2. (Previously Presented) The image sensor of claim 1 wherein said amplifier further includes a second input receiving said reset reference voltage signal.

Claim 3. (Previously Presented) The image sensor of claim 2 wherein said reset transistor includes a gate and first and second terminals, said first terminal connected to receive said negative feedback signal to adjust said second terminal's voltage to a selected reset voltage.

Claim 4. (Previously Presented) The image sensor of claim 3 wherein said reset reference voltage source signal is selected to control said voltage at said second reset transistor terminal to be about V_T -ΔV below a reset voltage applied at said gate terminal of said reset transistor, where V_T is a threshold voltage that is characteristic of said reset transistor, and ΔV is selected to maintain said reset transistor in a subthreshold region of operation during a steady state phase of pixel reset.

Claim 5. (Previously Presented) The image sensor of claim 4 wherein said selected ΔV is greater than about one hundred millivolts.

Claim 6. (Previously Presented) The image sensor of claim 4 wherein said select node of each said pixel comprises a terminal of a row select transistor that is coupled to said first input of said amplifier.

Claim 7. (Previously Presented) The image sensor of claim 6 wherein each said pixel further comprises a source follower transistor coupled between said second terminal of said reset transistor and a terminal of said row select transistor.

Claim 8. (Previously Presented) The image sensor of claim 3 wherein said first circuit comprises a photocircuit.

Claim 9. (Previously Presented) The image sensor of claim 8 wherein said amplifier comprises a differential amplifier including a first differential amplifier input transistor connected to receive said first amplifier input and a second differential amplifier input transistor connected to receive said second amplifier input, said first and second differential amplifier input transistors connected to provide a signal to a current mirror circuit that is connected to deliver said negative feedback signal to said reset transistor first terminal.

Claim 10. (Previously Presented) The image sensor of claim 8 wherein said photocircuit includes a photodiode and a capacitance.

Claim 11. (Previously Presented) The image sensor of claim 7 wherein said first circuit is a photocircuit.

Claim 12. (Previously Presented) The image sensor of claim 11 wherein said photocircuit includes a photodiode and a capacitance.

Claim 13. (Currently Amended) An image sensor array having rows and columns of pixels, comprising:

at least one column line;

a plurality of pixels each having an output, the outputs of pixels in a column being connected to a common respective column line, each said pixel including:

a first circuit that produces a signal proportional to incident light intensity, said first circuit being connected to supply said proportional signal to said pixel output, and

a reset transistor for resetting said pixel;

at least one amplifier, each said amplifier having a first input coupled to at least one said column line, each said amplifier being connected to provide a negative

feedback signal to each said pixel reset transistor of a respective column of pixels during each corresponding pixel reset phase; and

a reset reference voltage source connected to apply a reset reference voltage signal to each said amplifier to provide a voltage reference for controlling reset of said pixels.

Claim 14. (Previously Presented) The image sensor of claim 13 wherein said amplifier further includes a second input for receiving said reset reference voltage signal.

Claim 15. (Previously Presented) The image sensor of claim 14 wherein said reset transistor includes a gate and first and second terminals, said first terminal connected to receive said negative feedback signal to adjust said second terminal's voltage to a selected reset voltage.

Claim 16. (Previously Presented) The image sensor of claim 15 wherein said reset reference voltage source signal is selected to control said voltage at said second reset transistor terminal to be about V_T -ΔV below a reset voltage applied at said gate terminal of said reset transistor, where V_T is a threshold voltage that is characteristic of said reset transistor, and ΔV is selected to maintain said reset transistor in a subthreshold region of operation during a steady state phase of pixel reset.

Claim 17. (Previously Presented) The image sensor array of claim 16 wherein said selected ΔV is greater than about one hundred millivolts.

Claim 18. (Previously Presented) The image sensor array of claim 16 wherein each pixel comprises a row select transistor coupled between said second terminal of said reset transistor and said first input of said amplifier.

Claim 19. (Previously Presented) The image sensor array of claim 18 wherein each pixel further comprises a source follower transistor coupled between said second terminal of said reset transistor and a terminal of said row select transistor.

Claim 20. (Previously Presented) The image sensor array of claim 16 wherein said first circuit of each pixel comprises a photocircuit.

Claim 21. (Previously Presented) The image sensor array of claim 20 wherein said amplifier comprises a differential amplifier including a first differential amplifier input transistor connected to receive said first amplifier input and a second differential amplifier input transistor connected to receive said second amplifier input, said first and second differential amplifier input transistors connected to provide a signal to a current mirror circuit that is connected to deliver said negative feedback signal to said reset transistor first terminal.

Claim 22. (Previously Presented) The image sensor array of claim 20 wherein said photocircuit of each active pixel comprises a photodiode and a capacitance.

Claim 23. (Previously Presented) The image sensor array of claim 19 wherein each said first circuit comprises a photocircuit.

Claim 24. (Previously Presented) The image sensor array of claim 23 wherein each said photocircuit comprises a photodiode and a capacitance.

Claim 25. (Previously Presented) An image sensor array having rows and columns of pixels, comprising:

at least one row line;

a plurality of pixels each having an output, the outputs of pixels in a row being connected to a common respective row line, each said pixel including:

a first circuit that produces a current proportional to incident light intensity, said first circuit being connected to supply said proportional current to said pixel output, and

a reset transistor for resetting said pixel;

at least one amplifier, each said amplifier having a first input coupled to at least one said row line, each said amplifier being connected to provide a negative feedback signal to each said pixel reset transistor of a respective row ~~if~~ of pixels during each corresponding pixel reset phase; and

a reset reference voltage source connected to apply a reset reference voltage signal to each said amplifier to provide a voltage reference for controlling reset of said pixels.

Claim 26. (Previously Presented) The image sensor of claim 25 wherein said amplifier further includes a second input for receiving said reset reference voltage signal.

Claim 27. (Previously Presented) The image sensor of claim 26 wherein said reset transistor includes a gate and first and second terminals, said first terminal connected to receive said negative feedback signal to adjust said second terminal's voltage to a selected reset voltage.

Claim 28. (Previously Presented) The CMOS image sensor of claim 27 wherein said reset reference voltage source signal is selected to control said voltage at said second terminal to be about V_T -ΔV below a reset voltage applied at said gate terminal of said reset transistor, where V_T is a threshold voltage that is characteristic of said reset transistor, and ΔV is selected to maintain said reset transistor in a subthreshold region of operation during a steady state phase of pixel reset.

Claim 29. (Previously Presented) The image sensor array of claim 28 wherein said selected ΔV is greater than about one hundred millivolts.

Claim 30. (Previously Presented) The image sensor array of claim 28 wherein each pixel comprises a column select transistor coupled between said second terminal of said reset transistor and said first input of said amplifier.

Claim 31. (Previously Presented) The image sensor array of claim 30 wherein each pixel further comprises a source follower transistor coupled between said second terminal of said reset transistor and a terminal of said column select transistor.

Claim 32. (Previously Presented) The image sensor array of claim 28 wherein said first circuit of each pixel comprises a photocircuit.

Claim 33. (Previously Presented) The image sensor array of claim 32 wherein said amplifier comprises a differential amplifier including a first differential amplifier input transistor connected to receive said first amplifier input and a second differential amplifier input transistor connected to receive said second

amplifier input, said first and second differential amplifier input transistors connected to provide a signal to a current mirror circuit that is connected to deliver said negative feedback signal to said reset transistor first terminal.

Claim 34. (Previously Presented) The image sensor array of claim 32 wherein said photocircuit of each pixel comprises a photodiode and a capacitance.

Claim 35. (Previously Presented) The image sensor array of claim 31 wherein each said first circuit comprises a photocircuit.

Claim 36. (Previously Presented) The image sensor array of claim 35 wherein each said photocircuit comprises a photodiode and a capacitance.

Claim 37. (Previously Presented) The image sensor of claim 1 wherein said image sensor comprises a CMOS-compatible image sensor.

Claim 38. (Previously Presented) The image sensor array of either of claims 13 or 25 wherein said image sensor array comprises a CMOS-compatible image sensor array.

Claim 39. (Previously Presented) The image sensor of claim 1 wherein said pixels comprise active pixels.

Claim 40. (Previously Presented) The image sensor array or either of claims 13 or 25 wherein said pixels comprise active pixels.